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ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
TRA, ANH QUAN	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/820,556
Filing Date: April 08, 2004
Appellant(s): KIN LAW, OSCAR MING

Christopher P. Moreno
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/29/08 appealing from the Office action mailed 4/11/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6380764	Katoh et al.	04-2002
6774705	Miyazaki et al.	08-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7-10, 12-20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (USP 6380764) in view of Miyazaki et al. (USP 6774705), previously cited.

As to claim 1, Katoh et al.'s figure 12 shows a delay circuit (inv1 and inv2) having first and second computing devices, each of the computing devices having different one of a plurality of different threshold voltages. Figure 12 fails to teach circuit that controls the delay time of the delay circuit. However, Miyazaki et al.'s figure 14 shows a delay control circuit (all elements excepting LSI) having circuit MON that replicates the delay circuit LSI and the remaining circuits detect and adjust the delay of both LSI and MON circuit to provide a precise delay due to temperature/process variation. Therefore, it would have been obvious to one having ordinary skill in the art to use Miyazaki et al.'s delay control circuit to control the delay of Katoh et al.'s delay circuit (INV1 and INV2) in order to maintaining an accurate delay for circuits INV1 and INV2. Thus, the modified Katoh et al.'s figure 12 shows: a master controller (Miyazaki's OP and DCE); a dynamic voltage supplier (Miyazaki's VDDGEN); an adaptive body biaser (Miyazaki's VBBGEN); plurality of computing devices (Katoh's INV1 and INV2 in Miyazaki's MON), each of the computing devices having different one of plurality of different threshold voltages, connect and function as claimed.

As to claim 7, the modified Katoh's figure 12 shows that the master controller receives the operation state value from a processing device (circuit that generates Miyazaki's REF).

As to claim 8, the modified Katoh's figure 12 shows that the plurality of computing devices are disposed on a processing element.

As to claim 9, the modified Katoh's figure 12 shows that the supply voltage indicator and the body bias indicator are voltages.

Claims 10 and 12-19 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claims 20 and 23, the modified Katoh's figure 12 shows first and second sub-section (INV1 and INV2 in Miyazaki's MON), each sub-section includes a plurality of computing devices (PMOS and NMOS) having different one of a plurality of threshold voltages relative to the other sub-sections.

As to claim 24, the modified Katoh's figure 12 further shows that the plurality of computing devices comprises a first computing device (INV1) and a second computing device (INV2) comprises at least two transistor devices operatively coupled in a push-pull configuration, and an output of the first computing device is coupled to an input of the second computing device.

(10) Response to Argument

In response to the arguments in section (a), pages 16-17, Katoh may reject the teachings of the cited Japanese application and the IEEE Journal (col. 1, lines 53-65). However, Appellant does not show that the circuits in the Japanese application and the IEEE Journal are the same as Miyazaki's circuit. Katoh discloses that circuits in the Japanese application and the IEEE Journal respectively select a particular substrate voltage and a particular power supply voltage for a CMOS circuit in order to select different speeds for the

CMOS circuit in different operation modes or states. Katoh is silent about the influence of the variations in manufacturing process and operating temperature. In contrast, it is inherent and Miyazaki also discloses that the operation speed of any CMOS circuit is made variable depending on the variations in manufacturing process and operating temperature. Miyazaki teaches a circuit that is capable of compensating the speed variations or offset of CMOS delay circuit due to the variations in manufacturing process and operating temperature. Miyazaki's circuit constantly adjusts (within one mode or state) the substrate bias voltage and power supply voltage of a CMOS circuit in order to maintain a constant desired speed. Miyazaki also teaches that "low power consumption is realized without degrading the operating speed of the CMOS circuit or increasing the power consumption of the CMOS circuit" (abtract). Thus, Miyazaki's teaching is different from the teachings of the Japanese application and the IEEE Journal, and Miyazaki's teaching is not rejected by Katoh. One skilled in the art would be motivated to employ Miyazaki's teaching for Katoh's CMOS delay circuit in order to compensate the speed variation due to the variations in manufacturing process and operating temperature.

In response to the arguments in section (b), pages 17-18, Katoh only rejects the teaching of the Japanese application and the IEEE Journal respectively which select a particular substrate voltage and a particular power supply voltage for a CMOS circuit in order to select different speeds for the CMOS circuit in different modes or states. Miyazaki teaches a different circuit having different use and is not rejected by Katoh. Employing Miyazaki's teaching for Katoh would not change its basic operating principle, but would improve the circuit operation because the speed offset due to the variations in manufacturing process and operating temperature will be compensated.

In response to the arguments in section (c), page 19, Miyazaki teaches a single control circuit that is used to compensate the speed of plurality of inverters. Therefore, the duplication

of Miyazaki's control circuits is not needed in Katoh reference. Miyazaki's control circuit is not too complex for its delay. Thus, it is also not too complex for Katoh's delay. One skilled in the art would be motivated to employ Miyazaki's teaching for Katoh's CMOS delay circuit in order to compensate the speed variation due to the variations in manufacturing process and operating temperature.

In response to the arguments in section (d), pages 19-20, CMOS circuit operates with inaccurate speed due to temperature variation would cause operation error and increase manufacturing cost. Therefore, one skilled in the art would be motivated to use Miyazaki's teaching for Katoh's delay circuit in order to reduce operation error and manufacturing cost.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Lincoln Donovan /LD/

/Lincoln Donovan/

Supervisory Patent Examiner, Art Unit 2816

Drew A. Dunn
/D. A. D./
TQAS, TC 2800

/QUAN TRA/
Primary Examiner, Art Unit 2816